Code -

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END SEMESTER EXAMINATION

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Course Code : CSE204 **Course Name : Computer Organization and Architecture**

Marking Scheme and Solution

Q. 1		
	Solve any five	**Marks**
a)	Identification of component: Transistor Advantages (any 2)	1 1
b)	Amdahl's law: states that "the overall performance improvement gained by optimizing a single part of a system is limited by the fraction of time that the improved part is actually used". Speed up Equation: Amdahl's Law can be expressed in mathematically as follows – SpeedupMAX = 1/((1-p)+(p/s)) SpeedupMAX = maximum performance gain s = performance gain factor of p after implement the enhancements. p = the part which performance needs to be improved.	1 1
c)	Given: Mapping methods: 4 way set associative Cache size= 16KB=2^14 bytes 1 word=32 bits=4 bytes Block size (Offset)= 8 words * 4 bytes = 32 bytes= 2^5 bytes Physical address= 4GB=2^32 Bytes Block offset= 5 bits No. Of lines=cache size/block size= 2^14/2^5= 2^9 lines No. Of sets= No. Of lines/set size=2^9/2^2=2^7 Set no= 7 bits No. Of tag bits= total size of physical address - set no- offset = 32-(7+5)= 20 bits	1 1
d)	I/O module functions (any 4): Control and Timing, Processor communication, Device communication, data buffering, Error detection	2
e)	$(5655)_8$= 101110101101 By grouping of 4 bits from LSB to MSB hex no. Obtained Ans: BAD	1 1

f)	Represent the +384 in IEEE 32 bit floating point format Binary of 384=110000000 = 1.1 × 21000 Change binary exponent to biased exponent: 127 + 8 = 135 = 10000111 Format: 0 10000111 00000000000000000000000	1 1
g)	2's complement representation of -6 −6 11111010 +13 00001101 +7 00000111	1 1
h)	Given, LHS=A′.B+B.C′+B.C+A.B′. C′ A′B+(BC′+BC′)+BC+AB′C′ [By idempotent law, BC' = BC' + BC'] A′B+(BC′+BC)+(BC′+AB′C′) A′B+B(C′+C)+C′(B+AB′) [By distributive laws] A′B+B.1+C′(B+A) [(C′ + C) = 1 and absorption law (B + AB′)= (B + A)] B(A′+1)+C′(B+A) B.1+C′(B+A) [(A′ + 1) = 1] B+BC′+AC′ B(1+C′)+AC′ B + AC' =RHS Hence proved	1 1
Q.2	**Solve any two following questions**	8
a)	Need of GPU Applications of GPU	2 2
b)	Minimum 4 differentiating points	4
c)	Multi core architecture with diagram Working	2 2
Q.3	**Solve any two following questions**	8
a)	Identification of processor: ARM processor Justification	1 3
b)	Explanation min 4 points	4
c)	Two different compilers are being tested for a 500 MHz. machine with three different classes of instructions: A, B and C which requires 1, 2 and 3 cycles respectively.	

	Instruction Counts in billions		
Code from	A	B	C
Compiler-1	5	1	1
Compiler-2	10	1	1

a) Find CPU execution time and MIPS of both compilers. — 1

CPU Clock cycles$_1$ = (5 x 1 + 1 x 2 + 1 x 3) x 10^9 = 10 x 10^9

CPU Clock cycles$_2$ = (10 x 1 + 1 x 2 + 1 x 3) x 10^9 = 15 x 10^9 — 1

CPU time$_1$ = 10 x 10^9 / 500 x 10^6 = 20 seconds — 1

CPU time$_2$ = 15 x 10^9 / 500 x 10^6 = 30 seconds

MIPS$_1$ = (5 + 1 + 1) x 10^9 / 20 x 10^6 = 350

MIPS$_2$ = (10 + 1 + 1) x 10^9 / 30 x 10^6 = 400 — 1/2

b) Which sequence will be faster according to MIPS ?
Compiler 2 is faster — 1/2

c) Which sequence will be faster according to CPU time?
Compiler 1 faster

Q.4	**Solve any two following questions**	8
a)	Diagram of Direct Mapping Formula Explanation	1 1 2
b)	Justification	4
c)	Explanation with example	4
Q.5	**Solve any two following questions**	8
a)	Identification of I/O Technique: DMA Explanation	1 3
b)	Minimum 2 key features of Thunderbolt technology protocol stack diagram Explanation	2 1 1
c)	Each device techniques carry 2 marks	4
Q.6	**Solve any two following questions**	8
a)	1) 2560 Binary : 101000000000 HEX= A00	2

16	2560	
16	160	0
16	10	0
16	0	10

	2) 204.125 HEX: CC.2 16 | 2560 16 | 160 | 0 16 | 10 | 0 16 | 0 | 10 For Decimal Numbers **Decimal Number** — **Answer** — **Ineger Part** 0.125 x 16 = 2 — 2 Binary: 11001100.001 2 | 204 2 | 102 | 0 2 | 51 | 0 2 | 25 | 1 2 | 12 | 1 2 | 6 | 0 2 | 3 | 0 2 | 1 | 1 2 | 0 | 1 For Decimal Numbers Decimal Number — Answer Integer Part 0.125 x 2 = 0.25 0 0.25 x 2 = 0.5 0 0.5 x 2 = 1 1 Write the Integer part from top to bottom=001	1 1
b)	Hexadecimal to binary and decimal 1) A64 : Binary: 101001100100 Write equivalent binary for given hexadecimal value A64=101001100100 Decimal: $A64_{16} = (A \times 16^2) + (6 \times 16^1) + (4 \times 16^0)$ ANS: 2660 2) 1F.C :Binary:00011111.1100 Decimal: $1F.C_{16} = (1 \times 16^1) + (F \times 16^0) + (C \times 16^{-1})$ ANS: 31.75	1 1 1 1
c)	Programmable Logic Array Design of PLA	2 2

Paper Setter Signature