Code - 2030

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# Maharashtra Institute of Technology, Aurangabad

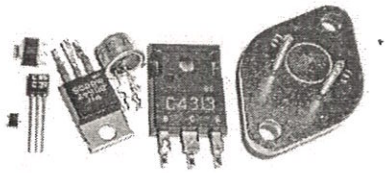
(An Autonomous Institute)

END SEMESTER EXAMINATION

## Second Year B.Tech (CSE) – Feb/Mar-2023

**Course Code : CSE204** **Course Name : Computer Organization and Architecture**
**Duration : 2 Hrs** **Max. Marks : 50** **Date :** 10 FEB 2023
**Instructions :**

**i) All questions are compulsory**
**ii) Assume suitable data wherever necessary and clearly state it**
**iii) Figures to right indicate full marks**

| Q. 1 | **Solve any five following questions** | | | | |
|---|---|---|---|---|---|
| | | **Marks** | **CO** | **BL** | **PI** |
| a) | Identify the following component? Write its any two advantages.   | 2 | 1 | 1 | 1.6.1 |
| b) | State Amdahl's law and explain its speedup equation. | 2 | 2 | 2 | 1.6.1 |
| c) | A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. Find number of bits for the TAG field? | 2 | 3 | 3 | 1.7.1 |
| d) | What are the major functions of I/O module? | 2 | 4 | 1 | 1.6.1 |
| e) | Convert the octal number 5655 in hexadecimal notation | 2 | 5 | 3 | 1.7.1 |
| f) | Represent the +384 in IEEE 32 bit floating point format | 2 | 6 | 3 | 1.7.1 |
| g) | Assume numbers are represented in 8-bit twos complement representation. Perform the following operation -6+13 | 2 | 6 | 2 | 1.7.1 |
| h) | Prove the following : $A'.B+B.C'+B.C+A.B'.C' = B + A.C'$ | 2 | 6 | 3 | 1.7.1 |
| **Q.2** | **Solve any two following questions** | 8 | | | |
| a) | Why GPU is needed? Explain with suitable applications. | 4 | 1 | 2 | 1.6.1 |
| b) | Differentiate between second generation and third generation of computers | 4 | 1 | 2 | 1.6.1 |
| c) | What do you mean by multi core architecture and how it | 4 | 1 | 2 | 1.6.1 |

| | | | | | |
|---|---|---|---|---|---|
| | works? | | | | |
| **Q.3** | **Solve any two following questions** | 8 | | | |
| a) | If you want to design washing machine which processor is more suitable for the application? Justify your answer | 4 | 2 | 2 | 1.6.1 |
| b) | In evolution of Intel x86 architecture, what is difference between Pentium and previous generation 80486? | 4 | 2 | 2 | 1.6.1 |
| c) | Two different compilers are being tested for a 500 MHz. machine with three different classes of instructions: A, B and C which requires 1, 2 and 3 cycles respectively.<br>**Instruction Counts in billions**<br>Code from \| A \| B \| C<br>Compiler-1 \| 5 \| 1 \| 1<br>Compiler-2 \| 10 \| 1 \| 1<br>a) Find CPU execution time and MIPS of both compilers.<br>b) Which sequence will be faster according to MIPS ?<br>c) Which sequence will be faster according to CPU time? | 4 | 2 | 3 | 1.7.1 |
| **Q.4** | **Solve any two following questions** | 8 | | | |
| a) | Explain Direct mapping cache organization with suitable diagram. | 4 | 3 | 2 | 1.6.1 |
| b) | How does synchronous DRAM differ from ordinary DRAM? Justify your answer. | 4 | 3 | 2 | 2.2.4 |
| c) | Write difference among EPROM, EEPROM, and flash memory. | 4 | 3 | 3 | 1.6.1 |
| **Q.5** | **Solve any two following questions** | 8 | | | |
| a) | Mr. Bob wants to move large volume of data which most I/O technique is more suitable? Explain its functioning in brief | 4 | 4 | 3 | 1.6.1 |
| b) | What are the key features of Thunderbolt technology? Explain its protocol stack in brief. | 4 | 4 | 2 | 1.6.1 |
| c) | In Interrupt driven I/O how does the processor identifies the requesting device? Explain any two device identification techniques. | 4 | 4 | 2 | 1.6.1 |
| **Q.6** | **Solve any two following questions** | 8 | | | |
| a) | Convert the following decimal number to binary and Hexadecimal notation<br>1) 2560 2) 204.125 | 4 | 5 | 3 | 1.7.1 |
| b) | Convert the following Hexadecimal to binary and decimal<br>1) A64 2) 1F.C | 4 | 5 | 3 | 1.7.1 |
| c) | Describe programmable Logic Array and Draw the | 4 | 6 | 2 | 1.6.1 |

| | | | | | |
|---|---|---|---|---|---|
| | structure of a PLA with three inputs (C, B, A) and four outputs (O0, O1, O2, O3) with the outputs defined as follows:<br>$O_0 = \overline{A}\,\overline{B}C + A\overline{B} + AB\overline{C}$<br>$O_1 = \overline{A}\,\overline{B}C + AB\overline{C}$<br>$O_2 = C$<br>$O_3 = A\overline{B} + AB\overline{C}$ | | | | |