Code -

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(An Autonomous Institute)

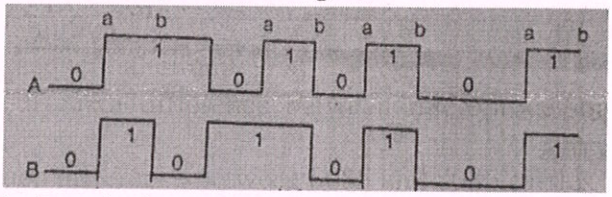
END SEMESTER EXAMINATION

Model Answer

Second Year B.Tech (CSE) – Feb/Mar-2023

Course Code : CSE203 **Course Name : Digital Electronics and Microprocessor**

Duration : 2 Hrs **Max. Marks : 50** **Date :**

	Answer/Solution	Stepwise Marking Scheme
Q.1	**Answer any five(Marks:10)**	
a)	Define what are basic logic gates and what are universal logic gates? **Answer:** Basic logic gate names and description Universal logic gate names and description	 1 Mark 1 Mark
b)	Compute two's complement of the number 01100111 **Answer:** Indication of process Final Answer	 1 Mark 1 Mark
c)	Convert the following expression into standard SOP form $Y = AB + A\bar{C}$ **Answer:** Multiplication with appropriate terms Final Answer representation	 1 Mark 1 Mark
d)	Draw and explain sequential circuit? **Answer:** Definition Diagram of sequential circuit	 1 Mark 1 Mark
e)	List any four main difference between microprocessor 8085 and 8086 **Answer:** Each difference between 8085 and 8086 carries ½ mark	 2 Mark
f)	Give the list of flags in 8086 **Answer:** Any four names of the flags	 2 Mark
g)	Define Addressing mode. **Answer:** Definition with appropriate wordings	 2 Mark
h)	Draw and Explain I/O mode of PPI 8255. **Answer:** I/O mode format Explaination	 1 Mark 1 Mark
Q.2	The input to a 2-input OR gate are pulses A and B of figure given below. Sketch the output pulse. Feed this output pulse as input to not gate and sketch the output of NOT gate.  **Answer:** Finding the input Sequence and writing To get output of OR gate with respect to input Sketch of OR output waveform To Provide NOT gate input and get output Sketch of NOT output waveform	 1 Mark 2 Mark 2 Mark 1 Mark 2 Mark
	OR	
Q.2	Explain commutative, associative, distributive laws and Duality theorem applied to Boolean algebra	

	Answer: commutative Law : Description Expression Associative Law : Description Expression Distributive Law : Description Expression Duality Theorem : Description Expression	1 Mark 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark
Q.3	Convert the following binary number 111000.0101 to a) Decimal b) Octal c) Hexadecimal D) Gray **Answer:** Decimal - Steps Answer Octal - Steps Answer Hexadecimal - Steps Answer Gray - Steps Answer	 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark 1 Mark
	OR	
Q.3	Elaborate what is meant by data select lines in multiplexer and demultiplexer? Discuss their role in data selection with example. **Answer:** Description for data select lines of MUX Description for data select lines of DEMUX Example of MUX Example of DEMUX	 2 Mark 2 Mark 2 Mark 2 Mark
Q.4	Simplify the logic function $Y=\sum m(1,5,6,7,11,12,13,15)$ Use Karnaugh map. Draw logic circuit for the simplified function **Answer:** Preparing K-Map with minterms representation Appropriate grouping Drawing the equation	 3 Mark 2 Mark 3 Mark
	OR	
Q.4	a) Explain the functions of the ALE signal and accumulator of the 8085 microprocessor **Answer:** ALE description ALE Waveform Accumulator functions Accumulator Input and output condition b) Describe memory segmentation. How it is done in 8086 microprocessor **Answer:** Diagram for memory segmentation Description for it	 1 Mark 1 Mark 1 Mark 1 Mark 2 Mark 2 Mark

Q.5	a) Calculate physical address when CS=4370H, IP=561EH
	Answer: Process indication
	Final answer
	
	b) Determine the content of register AL and the state of the flags. After the following instructions are executed.
	MOV AL,AB
	MOV BL,CD
	AND AL,BL
	Answer: Calculation of output
	Indication of flags affected
		
		2 Mark
		2 Mark
		
		2 Mark
		2 Mark

	OR	
Q.5	Two 16- bit numbers are stored at Data1 and Data2 respectively. Prepare an instruction sequence to Add, Subtract, AND these numbers and store it in Ans1,Ans2,Ans3 respectively. **Answer:** Flowchart Program with comment	 2 Mark 6 Mark
Q.6	A memory module of 16KB size is to be interfaced to 8086 microprocessor such that the memory address begins at 00000H. Use 4KB RAM chip. Specify i) Address decoding table ii) Chip select logic using 74LS138 decoder iii) Neat interfacing diagram **Answer:** Address decoding table Chip select logic using 74LS138 decoder Neat interfacing diagram	 2 Mark 2 Mark 4 Mark
	OR	
Q.6	Explain the following assembler directive in 8086 i. ASSUME ii. EQU iii. DW iv. DD **Answer:** Each assembler directive description carries 2 Mark	 8 Mark

Course Coordinator