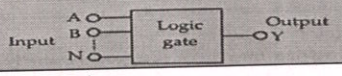
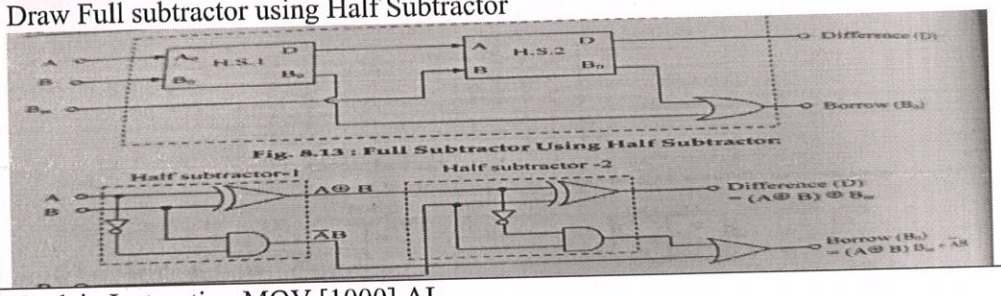
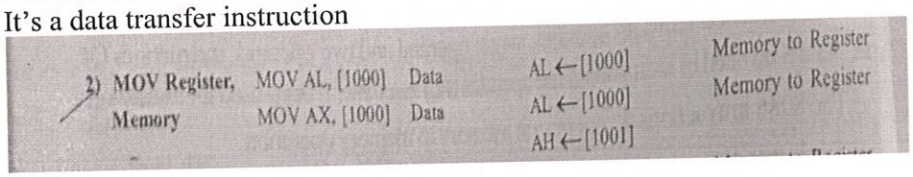
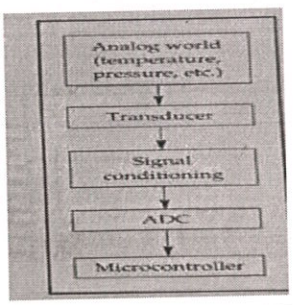
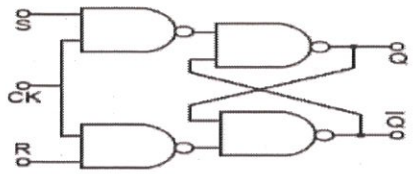
Q. 1	Solve any five following questions	Marks
a)	Define Boolean Algebra and draw block diagram of logic gate. To reduce or minimise any logic equations, mathematican *George Boolean* developed rules for manipulation of binary variables, known as *Boolean algebra*. By applying the rules of boolean algebra we can minimise the logic equation, which automatically reduces the hardware. Under this chapter we are going to study logic gates and boolean algebra. **4.2 Logic Gates :** The electronic or logic circuit having one or more than one inputs and only one output is called logic gate. The block diagram of logic gate is shown in fig. 4.1. 	(2) 1 1
b)	Draw Full subtractor using Half Subtractor  Fig. 8.13 : Full Subtractor Using Half Subtractor 	(2) 2
c)	Explain Instruction MOV [1000],AL ➔ It's a data transfer instruction  ➔	(2) 1 1
d)	Give Example of Arithmetic instructions ➢ Any one	(2) 2

OPCODE	OPERAND	EXPLANATION	EXAMPLE
ADD	D, S	D = D + S	ADD AX, [2050]
ADC	D, S	D = D + S + prev. carry	ADC AX, BX
SUB	D, S	D = D – S	SUB AX, [SI]
SBB	D, S	D = D – S – prev. carry	SBB [2050], 0050

e)	What is EEPROM? EEPROMis short for **"electrically erasable programmable read-only** memory." It's a flash drive memory device designed to retain the stored information even when the power is off.	(2) 2
f)	What is LM35, give steps to fetch data. The LM35 is a sensor that is capable of measuring temperature. 	(2) 1 1

g)	How much is data memory of 8051 ➢ 0000h ➢ To ffffh ➢ Explanation expected	(2) 1 1
h)	What are the addressing modes of 8051 > In 8051 There are six types of addressing modes. • Immediate AddressingMode • Register AddressingMode • Direct AddressingMode • Register IndirectAddressing Mode • Indexed AddressingMode • Implied AddressingMode	(2) 1 1
Q. 2	**Solve any two following questions**	
a)	Write truth table for three input Ex-OR gate with its applications. **Application of Ex-OR :** Some of the applications of Ex-OR gate is given below 1) It is used as magnitude compartor. 2) It is used in binary to gray code converter. 3) It is used in parity generator. 4) It is used in adder and subtractor circuits. > Input / Output A B C / Y 0 0 0 / 0 0 0 1 / 1 0 1 0 / 1 0 1 1 / 0 1 0 0 / 1 1 0 1 / 0 1 1 0 / 0 1 1 1 / 1 For three input Ex-OR gate	(4) 2 2
b)	Prove Associative laws using Truth table 4.3.1.5 Associative Laws : 1) A + (B + C) = (A + B) + C 2) A . (B . C) = (A . B) . C The associative law allows the group of variables and can be stated as " The grouping of any two terms of sum or any two factors of product does not affect the operation". Proof : The proof of above two laws are given in table 4.14 and table 4.15. The possible number of input combination is ($2^N = 2^3 = 8$) is eight. Table 4.14 A B C / A + (B + C) / (A + B) + C 0 0 0 / 0 / 0 0 0 1 / 1 / 1 0 1 0 / 1 / 1 0 1 1 / 1 / 1 1 0 0 / 1 / 1 1 0 1 / 1 / 1 1 1 0 / 1 / 1 1 1 1 / 1 / 1 These two columns are matching. There fore, A + (B + C) = (A + B) + C Table 4.15 A B C / A . (B . C) / (A . B) . C 0 0 0 / 0 / 0 0 0 1 / 0 / 0 0 1 0 / 0 / 0 0 1 1 / 0 / 0 1 0 0 / 0 / 0 1 0 1 / 0 / 0 1 1 0 / 0 / 0 1 1 1 / 1 / 1 These two columns are matching. There fore, A . (B . C) = (A . B) . C	4 2 2

c)	Reduce the following expression using Boolean algebra ,implement the simplified form using NAND Gates Y=AB+$\overline{AC}$+ A$\bar{B}C(AB+C)$ > vi) $\overline{(AB+C)}+(\overline{A}\,\overline{B}+\overline{C})$ Answer : i) $Y = AB+\overline{AC}+A\bar{B}C(AB+C)$ $= AB+\overline{AC}+A\bar{B}C.AB+A\bar{B}C.C$ (Distributive Law) $= AB+\overline{AC}+0+A\bar{B}C$ (AND Law) $= AB+\overline{AC}+A\bar{B}C$ (OR Law) $= A(B+\bar{B}C)+\overline{AC}$ (Distributive Law) $= A(B+C)+\overline{AC}$ (Other Law $B+\bar{B}C=B+C$) $= AB+AC+\overline{AC}$ (Distributive Law) $= AB+AC+\overline{A}+\overline{C}$ (Demorgan's Law) $= AB+\overline{A}+C+\overline{C}$ (Other Law $\overline{A}+AC=\overline{A}+C$) $= AB+\overline{A}+1$ (OR Law $C+\overline{C}=1$) $Y = 1$ (OR Law $1+\overline{A}+AB=1$) Logic 0 — Y = 1	(4) 3 1
Q. 3	**Solve any two following questions**	
a)	Simplify the following three variable logic expression Y= ΠM(1,3,5) **Ex. 7.5.4 :** Simplify the following three variable logic expression. $Y = \Pi M(1, 3, 5)$ **Soln. :** The given expression can be expressed in terms of maxterms as, $Y = M_1 \cdot M_3 \cdot M_5 = (A+B+\overline{C})(A+\overline{B}+\overline{C})(\overline{A}+B+\overline{C})$ **Step 1 : Bring the expression into SOP form.** $\therefore Y = (A+B+\overline{C})(A+\overline{B}+\overline{C})(\overline{A}+B+\overline{C})$ $= (A+B+\overline{C})(A\overline{A}+AB+A\overline{C}+\overline{A}\,\overline{B}+\overline{B}B+\overline{B}\,\overline{C}+\overline{A}\,\overline{C}+B\overline{C}$ **Step 2 : Simplify** But $A\overline{A}=0$, $\overline{B}B=0$ and $\overline{C}\,\overline{C}=\overline{C}$ $\therefore Y = (A+B+\overline{C})(AB+A\overline{C}+\overline{A}\,\overline{B}+\overline{B}\overline{C}+\overline{A}\,\overline{C}+B\overline{C}+\overline{C})$ $= (A+B+\overline{C})[AB+A\overline{C}+\overline{A}\,\overline{C}+\overline{A}\,\overline{B}+\overline{B}\overline{C}+B\overline{C}+\overline{C}]$ $= (A+B+\overline{C})[AB+\overline{C}(A+\overline{A})+\overline{A}\,\overline{B}+\overline{C}(\overline{B}+B)+\overline{C}]$ But $(A+\overline{A})=1$, $(\overline{B}+B)=1$ $\therefore Y = (A+B+\overline{C})[AB+\overline{C}+\overline{A}\,\overline{B}+\overline{C}+\overline{C}]$ But $\overline{C}+\overline{C}=\overline{C}$ $\therefore Y = (A+B+\overline{C})(AB+\overline{A}\,\overline{B}+\overline{C}+\overline{C}] = (A+B+\overline{C})(AB+\overline{A}\,\overline{B}+\overline{C})$ $= AAB+A\overline{A}\,\overline{B}+A\overline{C}+AB\overline{B}+\overline{A}\,\overline{B}B+B\overline{C}+AB\overline{C}+\overline{A}\,\overline{B}\overline{C}+\overline{C}\overline{C}$ But $AAB=AB$, $A\overline{A}\,\overline{B}=0$, $AB\overline{B}=AB$, $\overline{A}\,\overline{B}B=0$ and $\overline{C}\,\overline{C}=\overline{C}$ $\therefore Y = AB+A\overline{C}+AB+B\overline{C}+AB\overline{C}+\overline{A}\,\overline{B}\overline{C}+\overline{C}$ But $AB+AB=AB$ $\therefore Y = AB+A\overline{C}+B\overline{C}+AB\overline{C}+\overline{A}\,\overline{B}\overline{C}+\overline{C}$ $= AB+AB\overline{C}+A\overline{C}+B\overline{C}+\overline{A}\,\overline{B}\overline{C}+\overline{C}$ $= AB(1+\overline{C})+A\overline{C}+B\overline{C}+\overline{A}\,\overline{B}\overline{C}+\overline{C}$ $= AB+A\overline{C}+B\overline{C}+\overline{A}\,\overline{B}\overline{C}+\overline{C}$ ....since $(1+\overline{C})=1$ $= AB+\overline{C}(A+B+\overline{A}\,\overline{B}+1)$ $\therefore Y = AB+\overline{C}$ ....since $(A+B+\overline{A}\,\overline{B}+1)=1$	(4) 2 2
b)	List out types of Flip-flops and explain SR Flip flop. > Flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates. **Types of flip-flops:** 1. RS Flip Flop 2. JK Flip Flop 3. D Flip Flop 4. T Flip Flo	(4) 1 1



TRUTH TABLE

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

1

1

c) Minimize following logic function using K-maps and realize using the basic gate (4)
F(A,B,C,D)=Σm(0,1,2,3,7,8,9,10,11,12,13)
>

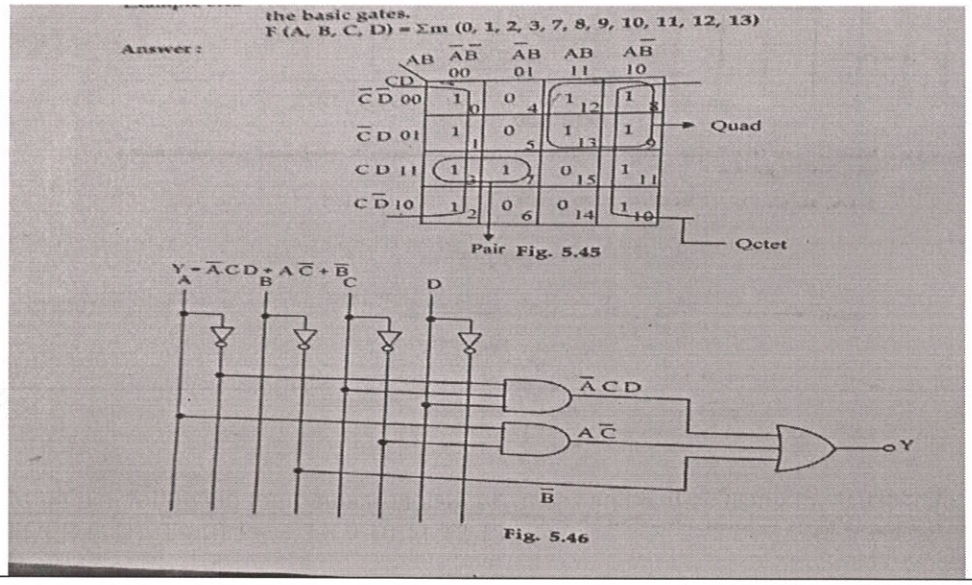


Fig. 5.46

3

1

Q. 4 **Solve any two following questions**

a) State the features of microprocessor 8086. (any six) (4)
>

1.2 Features of 8086

1) It operates on single +5 V power supply. 1

2) The 8086 has 20 bit address lines, hence it can address 1M byte memory locations. 1

3) It operates with 5 MHz clock frequency. 1

4) The 6 byte queue is used in 8086 to speed up instructions execution. 1

5) It has 16 bit multiplexed address/data bus, which reduces the number of pins. 1

6) The 8086 performs arithmetic and logical operations on bit, byte, word including multiply and divide operations. 1

7) The 8086 can generate 16 bit I/O address hence it can access $2^{16} = 65535$ I/O ports.
8) The 8086 work with register, direct, immediate, register indirect, based and indexed addressing modes.
9) The 8086 operates in minimum mode and maximum mode. When one microprocessor is used in system, the 8086 operates in the minimum mode. When two or more processors are used, it operates in maximum mode.
10) The 8086 supports multiprogramming.
11) It provides 16 bit registers as AX, BX, CX, DX, index register SI and DI, base pointer BP and stack pointer SP.
12) It consists of four segments CS (Code Segment), DS (Data Segment), ES (Extra Segment) and SS (Stack Segment).
13) The 8086 flag register contains 9 flags. The conditional flags are SF (Sign Flag), CF (Carry Flag), ZF (Zero Flag), PF (Parity Flag), OF (Overflow Flag) and AF (Auxiliary Flag). The control flags are TF (Trap Flag), DF (Direction Flag) and IF (Interrupt Flag).

1.3 8086 Internal Architecture

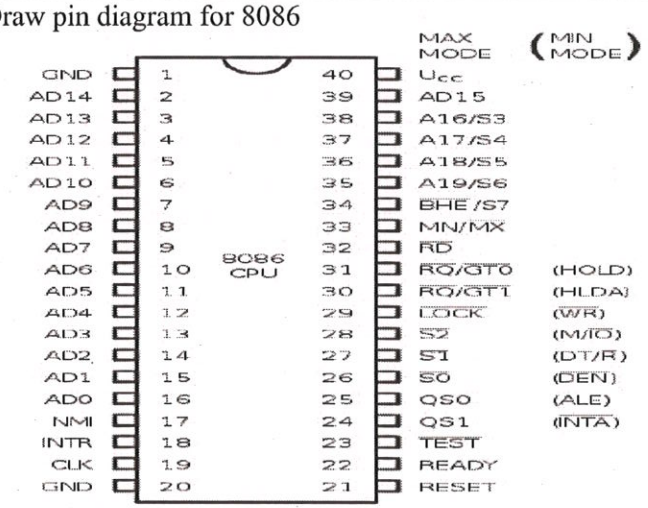
b) List out addressing mode of 8086 — (4)

>

There are eight addressing modes in 8086 MPU. These modes are:

- Immediate Addressing Mode — 1
- Register Addressing Mode — 1
- Direct Addressing Mode — 1
- Register Indirect Addressing Mode — 1
- Based Addressing Mode
- Indexed Addressing Mode
- Based-Index Addressing Mode
- Based-Index with displacement addressing mode

c) Draw pin diagram for 8086 — (4)



Brief info expected — 3 + 1

Q. 5	**Solve any two following questions**

a) State the Operating Modes of 8086 with brief information about pins. — (4)

There are two operating modes of operation for Intel 8086, namely the **minimum mode** and the **maximum mode**. — 1

When only one 8086 CPU is to be used in a microprocessor system, the 8086 is used in the **Minimum mode** of operation.

Pin Description for Minimum Mode

In this minimum mode of operation, the pin MN/$\overline{MX}$ is connected to 5V D.C. supply i.e. MN/$\overline{MX}$ = VCC. — 1

The description about the pins from 24 to 31 for the minimum mode is as follows:

INTA (Output): Pin number 24 interrupts acknowledgement. On receiving interrupt signal, the processor issues an interrupt acknowledgment signal. It is active LOW.

ALE (Output): Pin no. 25. Address latch enable. It goes HIGH during T1. The microprocessor 8086 sends this signal to latch the address into the Intel 8282/8283 latch. 1

DEN (Output): Pin no. 26. Data Enable. When Intel 8287/8286 octal bus transceiver is used this signal. It is active LOW.

DT/R (output): Pin No. 27 data Transmit/Receives. When Intel 8287/8286 octal bus transceiver is used this signal controls the direction of data flow through the transceiver. When it is HIGH, data is sent out. When it is LOW, data is received.

M/IO (Output): Pin no. 28, Memory or I/O access. When this signal is HIGH, the CPU wants to access memory. When this signal is LOW, the CPU wants to access I/O device.

WR (Output): Pin no. 29, Write. When this signal is LOW, the CPU performs memory or I/O write operation.

HLDA (Output): Pin no. 30, Hold Acknowledgment. It is sent by the processor when it receives HOLD signal. It is active HIGH signal. When HOLD is removed HLDA goes LOW.

HOLD (Input): Pin no. 31, Hold. When another device in microcomputer system wants to use the address and data bus, it sends HOLD request to CPU through this pin. It is an active HIGH signal.

Pin Description for Maximum Mode

In the maximum mode of operation, the pin MN/$\overline{MX}$ is made LOW. It is grounded. 1

b) Explain in brief Push and Pop Instruction (4)

LE10 PUSH and POP Instruction result (ZF = 0).

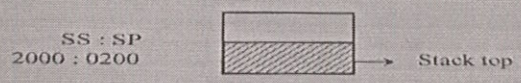
The stack is some part of RAM area set aside to store return addresses for subroutine calls, processor status after interrupt before going to ISR (interrupt service routine) and also to store the contents of register which may be changed or destroyed by the subroutine. 1

The stack is a 64 K byte memory whose base address is determined by the SS segment register. Two CPU registers normally point into this area. These are SP and BP.

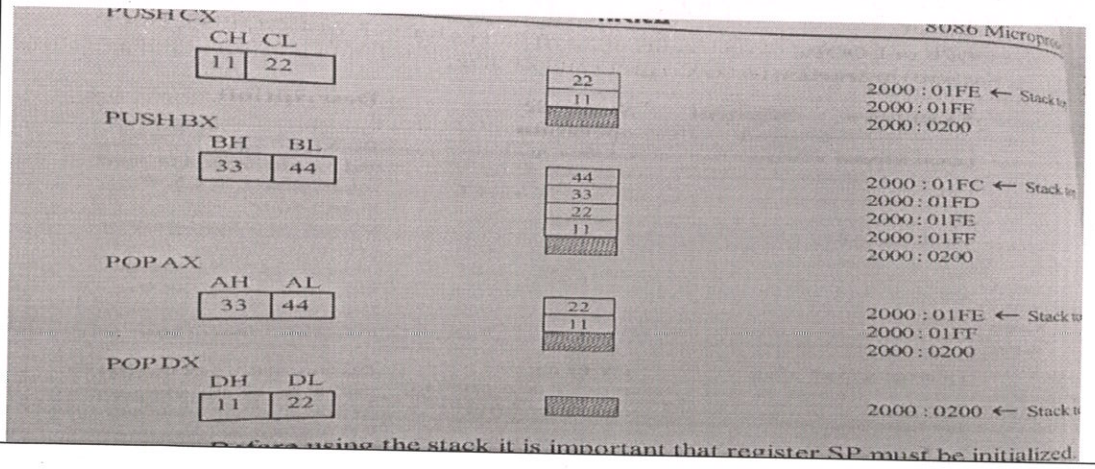
The stack is not another data segment but a special area in a memory used by the processor for temporary data storage.

The instruction related to stack are PUSH and POP instruction. The PUSH source instruction is used to store the content of register into stack and POP destinatin instruction causes the data currently on top of stack to be popped into the destination operand. The operations of PUSH & POP instructions are explained in the following example. The SP all the time point to the top of stack (TOS), means to the last entry pushed on the stack. 1

For example :



Assume that stack pointer is initialised with SS = 2000H and SP = 0200H. The effective address of stack is 20000 + 0200 = 20200 H.



1

1

Before using the stack it is important that register SP must be initialized.

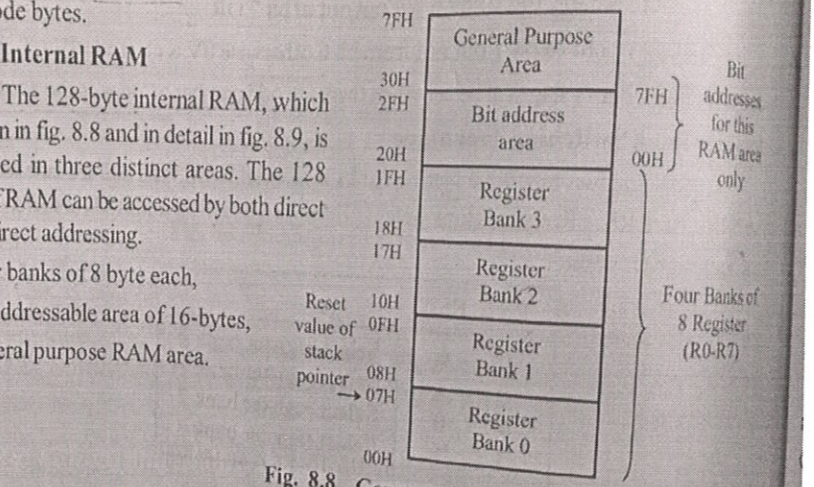
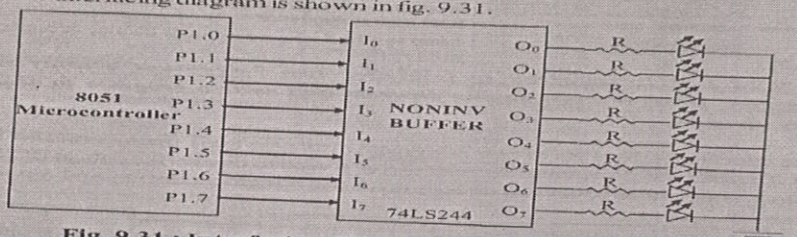
c) Write program for 8 bit Addition in 8086 (4)

```
;8 Bit addition

DATA SEGMENT                                   1
NUM1 DB 85H
NUM2 DB 92H                                    1
RESULT DB ?
DATA ENDS

CODE SEGMENT
START: ASSUME CS:CODE, DS:DATA
    MOV AX,DATA
    MOV DS,AX

    MOV AL,NUM1
    MOV BL,NUM2
    ADD AL,BL
    MOV RESULT,AL                              1

    MOV AH,4CH
    INT 21H

    END START
    CODE ENDS                                  1
```

Q. 6 Solve any two following questions

a) Write difference between microprocessor and microcontroller (any six) (4)

Microprocessor	**Microcontroller**	
Microprocessor is the heart of Computer system.	Micro Controller is the heart of an embedded system.	1
It is only a processor, so memory and I/O components need to be connected externally	Micro Controller has a processor along with internal memory and I/O components.	
Memory and I/O has to be connected externally, so the circuit becomes large.	Memory and I/O are already present, and the internal circuit is small.	1
You can't use it in compact systems	You can use it in compact systems.	1
Cost of the entire system is high	Cost of the entire system is low	
Due to external components, the total power consumption is high. Therefore, it is not ideal for the devices running on stored power like batteries.	As external components are low, total power consumption is less. So it can be used with devices running on stored power like batteries.	1
Most of the microprocessors do not have power saving features.	Most of the microcontrollers offer power-saving mode.	
It is mainly used in personal computers.	It is used mainly in a washing machine, MP3 players, and embedded systems.	
Microprocessor has a smaller number of registers, so more operations are memory-based.	Microcontroller has more register. Hence the programs are easier to write.	
Microprocessors are based on Von Neumann model	Micro controllers are based on Harvard architecture	
It is a central processing unit on a single silicon-based integrated chip.	It is a byproduct of the development of microprocessors with a CPU along with other peripherals.	
It has no RAM, ROM, Input-Output units, timers, and other peripherals on the chip.	It has a CPU along with RAM, ROM, and other peripherals embedded on a single chip.	
It uses an external bus to interface to RAM, ROM, and other peripherals.	It uses an internal controlling bus.	
Microprocessor-based systems can run at a very high speed because of the technology involved.	Microcontroller based systems run up to 200MHz or more depending on the architecture.	
It's used for general purpose applications that allow you to handle loads of data.	It's used for application-specific systems.	
It's complex and expensive, with a large number of instructions to process.	It's simple and inexpensive with less number of instructions to process.	

b)	Give generalize structure of internal RAM of 8051	(4)
	The 8051 has internal RAM of 128 bytes and internal ROM of 4K bytes. The RAM is used to store variable data that can be altered as the program runs. The ROM is used to store code bytes.	2
	8.2.5.1 Internal RAM The 128-byte internal RAM, which is shown in fig. 8.8 and in detail in fig. 8.9, is organised in three distinct areas. The 128 bytes of RAM can be accessed by both direct and indirect addressing. 1) Four banks of 8 byte each, 2) Bit addressable area of 16-bytes, 3) General purpose RAM area.	2
	 Fig. 8.8 Generalised Structure of Internal RAM	
c)	Draw interfacing diagram of 8 LED to 8051,also write program to blink 8 LED.	(4)
	Answer : The interfacing diagram is shown in fig. 9.31.	2
	 Fig. 9.31 : Interfacing of 8 LEDs to 8051 microcontroller	

	ALP:
	START MOV P1, #00H ; Port 1 as output port.
	MOV A, #FFH ;Data FFH for LED ON
	MOV P1, A ; LED ON
	LCALL DELAY ; Call a delay subroutine
	MOV A, #00H ; Data 00H for LED OFF
	MOV P1, A ; LED OFF
	LCALL DELAY ; Call a delay subroutine
	LJMP START ; Jump to START for continuous ON and OFF LED
	DELAY Subroutine
	LOOP MOV R1, #FFH ;Count 1 = $(255)_{10} = (FF)_{16}$
	UP MOV R2, #FFH ;Count 2 = $(255)_{10} = (FF)_{16}$
	DJNZ R2, UP ; If R2 ≠ 00H, Jump to UP
	DJNZ R1, LOOP ; If R1 ≠ 00H, Jump to LOOP
	RET ; Return from subroutine
		2